Contents

Chapter 1: nRF52832 Rev 1 Errata ................................................................. 4

Chapter 2: Change log ................................................................................. 5

Chapter 3: New and inherited anomalies .................................................. 7

3.1 [12] COMP: Reference ladder is not correctly calibrated .................. 8
3.2 [15] POWER: RAM[x].POWERSET/CLR read as zero ....................... 9
3.3 [20] RTC: Register values are invalid ................................................. 9
3.4 [31] CLOCK: Calibration values are not correctly loaded from FICR at reset 10
3.5 [36] CLOCK: Some registers are not reset when expected .................. 10
3.6 [51] I2S: Aligned stereo slave mode does not work ......................... 11
3.7 [54] I2S: Wrong LRCK polarity in Aligned mode ............................. 11
3.8 [55] I2S: RXPTRUPD and TXPTRUPD events asserted after STOP ........ 12
3.9 [58] SPI: An additional byte is clocked out when RXD.MAXCNT = 1 ...... 12
3.10 [64] NFC: Only full bytes can be received or transmitted, but supports 4-bit frame transmit .......................................................... 13
3.11 [66] TEMP: Linearity specification not met with default settings ........ 14
3.12 [67] NFC, PPI: Some events cannot be used with the PPI ................. 14
3.13 [68] CLOCK: EVENTS_HFCLKSTARTED can be generated before HFCLK is stable 15
3.14 [72] NFC, PPI: TASKS_ACTIVATE cannot be used with the PPI ....... 16
3.15 [74] SAADC: Started events fires prematurely ............................... 16
3.16 [75] MWU: Increased current consumption ...................................... 16
3.17 [76] LPCOMP: READY event is set sooner than it should ............... 17
3.18 [77] CLOCK: RC oscillator is not calibrated when first started ........ 17
3.19 [78] TIMER: High current consumption when using timer STOP task only 18
3.20 [79] NFC: A false EVENTS_FIELDDETECTED event occurs after the field is lost .... 18
3.21 [81] GPIO: PIN_CNFI is not retained when in debug interface mode .... 19
3.22 [83] TWI: STOPPED event occurs twice if the STOP task is triggered during a transaction ............................................................. 19
3.23 [84] COMP: ISOURCE not functional .................................................. 19
3.24 [86] SAADC: Triggering START task after offset calibration may write a sample to RAM 20
3.25 [87] CPU: Unexpected wake from System ON Idle when using FPU .... 20
3.26 [88] WDT: Increased current consumption when configured to pause in System ON idle .... 21
3.27 [89] TWI: Static 400 µA current while using GPIO0 .......................... 21
3.29 [97] GPIO: High current consumption in System ON Idle mode ......... 22
3.30 [101] CLOCK: Sleep current increases after soft reset ..................... 23
3.31 [102] RADIO: PAYLOAD/END events delayed or not triggered after ADDRESS .... 23
3.32 [106] RADIO: Higher CRC error rates for some access addresses ....... 24
3.33 [107] RADIO: Immediate address match for access addresses containing MSBs 0x0 .... 24
3.34 [108] RAM: RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode ............................................... 25
3.35 [109] DMA: DMA access transfers might be corrupted ................. 26
3.36 [113] COMP: Single-ended mode with external reference is not functional 26
3.37 [132] CLOCK: The LFRC oscillator might not start ......................... 26
3.38 [136] System: Bits in RESETREAS are set when they should not be .... 27
3.39 [138] RADIO: Spurious emission on GPIO exceeds limits in radiated tests .... 27
3.40 [141] NFCT: HFCLK not stopped when entering SENSE mode

3.41 [143] RADIO: False CRC failures on specific addresses

3.42 [146] CLOCK: LFRC frequency deviation

3.43 [149] TWIM: First clock pulse after clock stretching may be too long or too short

3.44 [150] SAADC: EVENT_STARTED does not fire

3.45 [155] GPIOTE: IN event may occur more than once on input edge

3.46 [156] GPIOTE: Some CLR tasks give unintentional behavior

3.47 [163] FICR: Code and RAM size fields do not match chip specification
Chapter 1
nRF52832 Rev 1 Errata

This Errata document contains anomalies for the nRF52832 chip, revision Rev 1 (QFAA-B00, QFAB-B00, CIAA-B00).

The document indicates which anomalies are fixed, inherited, or new compared to revision Engineering C.
# Chapter 2

## Change log

See the following list for an overview of changes from previous versions of this document.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>nRF52832</td>
<td>12.07.2017</td>
<td>  • Updated: No. 12. “Reference ladder is not correctly calibrated”</td>
</tr>
<tr>
<td>Rev 1 v1.6</td>
<td></td>
<td>  • Updated: No. 66. “Linearity specification not met with default settings”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Updated: No. 79. “A false EVENTS_FIELDDETECTED event occurs after the field is lost”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 102. “PAYLOAD/END events delayed or not triggered after ADDRESS”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 106. “Higher CRC error rates for some access addresses”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 107. “Immediate address match for access addresses containing MSBs 0x00”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 143. “False CRC failures on specific addresses”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 149. “First clock pulse after clock stretching may be too long or too short”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 155. “IN event may occur more than once on input edge”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 156. “Some CLR tasks give unintentional behavior”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 163. “Code and RAM size fields do not match chip specification”</td>
</tr>
<tr>
<td>nRF52832</td>
<td>21.04.2017</td>
<td>  • Updated: No. 136. “Bits in RESETREAS are set when they should not be”</td>
</tr>
<tr>
<td>Rev 1 v1.5</td>
<td></td>
<td>  • Added: No. 146. “LFRC frequency deviation”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 150. “EVENT_STARTED does not fire”</td>
</tr>
<tr>
<td>nRF52832</td>
<td>12.01.2017</td>
<td>  • Updated the attachment of No. 109. “DMA access transfers might be corrupted”</td>
</tr>
<tr>
<td>Rev 1 v1.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>nRF52832</td>
<td>16.12.2016</td>
<td>  • Added: No. 101. “Sleep current increases after soft reset”</td>
</tr>
<tr>
<td>Rev 1 v1.3</td>
<td></td>
<td>  • Added: No. 109. “DMA access transfers might be corrupted”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 113. “Single-ended mode with external reference is not functional”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 132. “The LFRC oscillator might not start”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 136. “Bits in RESETREAS are set when they should not be”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 138. “Spurious emission on GPIO exceeds limits in radiated tests”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 141. “HFCLK not stopped when entering SENSE mode”</td>
</tr>
<tr>
<td>nRF52832</td>
<td>28.09.2016</td>
<td>  • Added: No. 108. “RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode”</td>
</tr>
<tr>
<td>Rev 1 v1.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>nRF52832</td>
<td>05.07.2016</td>
<td>  • Added: No. 84. “ISOURCE not functional”</td>
</tr>
<tr>
<td>Rev 1 v1.1</td>
<td></td>
<td>  • Added: No. 86. “Triggering START task after offset calibration may write a sample to RAM”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>  • Added: No. 87. “Unexpected wake from System ON Idle when using FPU”</td>
</tr>
<tr>
<td>Version</td>
<td>Date</td>
<td>Change</td>
</tr>
<tr>
<td>-----------------</td>
<td>--------</td>
<td>----------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
</tbody>
</table>
| nRF52832        | 17.02.2016 | • Added: No. 12. “Reference ladder is not correctly calibrated”  
• Added: No. 15. “RAM[x].POWERSET/CLR read as zero”  
• Added: No. 20. “Register values are invalid”  
• Added: No. 31. “Calibration values are not correctly loaded from FICR at reset”  
• Added: No. 36. “Some registers are not reset when expected”  
• Added: No. 51. “Aligned stereo slave mode does not work”  
• Added: No. 54. “Wrong LRCK polarity in Aligned mode”  
• Added: No. 55. “RXPTRUPD and TXPTRUPD events asserted after STOP”  
• Added: No. 58. “An additional byte is clocked out when RXD.MAXCNT = 1”  
• Added: No. 64. “Only full bytes can be received or transmitted, but supports 4-bit frame transmit”  
• Added: No. 66. “Linearity specification not met with default settings”  
• Added: No. 67. “Some events cannot be used with the PPI”  
• Added: No. 68. “EVENTS_HFCLKSTARTED can be generated before HFCLK is stable”  
• Added: No. 72. “TASKS_ACTIVATE cannot be used with the PPI”  
• Added: No. 74. “Started events fires prematurely”  
• Added: No. 75. “Increased current consumption”  
• Added: No. 76. “READY event is set sooner than it should”  
• Added: No. 77. “RC oscillator is not calibrated when first started”  
• Added: No. 78. “High current consumption when using timer STOP task only”  
• Added: No. 79. “A false EVENTS_FIELDDETECTED event occurs after the field is lost”  
• Added: No. 81. “PIN_CNF is not retained when in debug interface mode”  
• Added: No. 83. “STOPPED event occurs twice if the STOP task is triggered during a transaction”  
| nRF52832        | 17.02.2016 | • Added: No. 88. “Increased current consumption when configured to pause in System ON idle”  
• Added: No. 89. “Static 400 µA current while using GPIOTE”  
• Added: No. 91. “Radio performance using CSP package version”  
• Added: No. 97. “High current consumption in System ON Idle mode”  
| nRF52832        | 17.02.2016 | • Added: No. 12. “Reference ladder is not correctly calibrated”  
• Added: No. 15. “RAM[x].POWERSET/CLR read as zero”  
• Added: No. 20. “Register values are invalid”  
• Added: No. 31. “Calibration values are not correctly loaded from FICR at reset”  
• Added: No. 36. “Some registers are not reset when expected”  
• Added: No. 51. “Aligned stereo slave mode does not work”  
• Added: No. 54. “Wrong LRCK polarity in Aligned mode”  
• Added: No. 55. “RXPTRUPD and TXPTRUPD events asserted after STOP”  
• Added: No. 58. “An additional byte is clocked out when RXD.MAXCNT = 1”  
• Added: No. 64. “Only full bytes can be received or transmitted, but supports 4-bit frame transmit”  
• Added: No. 66. “Linearity specification not met with default settings”  
• Added: No. 67. “Some events cannot be used with the PPI”  
• Added: No. 68. “EVENTS_HFCLKSTARTED can be generated before HFCLK is stable”  
• Added: No. 72. “TASKS_ACTIVATE cannot be used with the PPI”  
• Added: No. 74. “Started events fires prematurely”  
• Added: No. 75. “Increased current consumption”  
• Added: No. 76. “READY event is set sooner than it should”  
• Added: No. 77. “RC oscillator is not calibrated when first started”  
• Added: No. 78. “High current consumption when using timer STOP task only”  
• Added: No. 79. “A false EVENTS_FIELDDETECTED event occurs after the field is lost”  
• Added: No. 81. “PIN_CNF is not retained when in debug interface mode”  
• Added: No. 83. “STOPPED event occurs twice if the STOP task is triggered during a transaction”  

Doc. ID 4397_565 v1.6
Chapter 3
New and inherited anomalies

The following anomalies are present in revision Rev 1 of the nRF52832 chip.

**Table 1: New and inherited anomalies**

<table>
<thead>
<tr>
<th>ID</th>
<th>Module</th>
<th>Description</th>
<th>New in Rev 1</th>
<th>Inherited from Engineering</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>COMP</td>
<td>Reference ladder is not correctly calibrated</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>POWER</td>
<td>RAM[x].POWERSET/CLR read as zero</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>RTC</td>
<td>Register values are invalid</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>CLOCK</td>
<td>Calibration values are not correctly loaded from FICR at reset</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>CLOCK</td>
<td>Some registers are not reset when expected</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>I2S</td>
<td>Aligned stereo slave mode does not work</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>54</td>
<td>I2S</td>
<td>Wrong LRCK polarity in Aligned mode</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>I2S</td>
<td>RXPTRUPD and TXPTRUPD events asserted after STOP</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>SPIM</td>
<td>An additional byte is clocked out when RXD.MAXCNT = 1</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>NFCT</td>
<td>Only full bytes can be received or transmitted, but supports 4-bit frame transmit</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>66</td>
<td>TEMP</td>
<td>Linearity specification not met with default settings</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>67</td>
<td>NFCT,PPI</td>
<td>Some events cannot be used with the PPI</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>68</td>
<td>CLOCK</td>
<td>EVENTS_HFCLKSTARTED can be generated before HFCLK is stable</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>72</td>
<td>NFCT,PPI</td>
<td>TASKS_ACTIVATE cannot be used with the PPI</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>74</td>
<td>SAADC</td>
<td>Started events fires prematurely</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>75</td>
<td>MWU</td>
<td>Increased current consumption</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>76</td>
<td>LPCOMP</td>
<td>READY event is set sooner than it should</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>77</td>
<td>CLOCK</td>
<td>RC oscillator is not calibrated when first started</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>78</td>
<td>TIMER</td>
<td>High current consumption when using timer STOP task only</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>79</td>
<td>NFCT</td>
<td>A false EVENTS_FIELDDETECTED event occurs after the field is lost</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>81</td>
<td>GPIO</td>
<td>PIN_CNF is not retained when in debug interface mode</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>83</td>
<td>TWIS</td>
<td>STOPPED event occurs twice if the STOP task is triggered during a transaction</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>84</td>
<td>COMP</td>
<td>ISOURCE not functional</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>
### 3.1 [12] COMP: Reference ladder is not correctly calibrated

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

<table>
<thead>
<tr>
<th>ID</th>
<th>Module</th>
<th>Description</th>
<th>New in Rev 1</th>
<th>Inherited from Engineering C</th>
</tr>
</thead>
<tbody>
<tr>
<td>86</td>
<td>SAADC</td>
<td>Triggering START task after offset calibration may write a sample to RAM</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>87</td>
<td>CPU</td>
<td>Unexpected wake from System ON Idle when using FPU</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>88</td>
<td>WDT</td>
<td>Increased current consumption when configured to pause in System ON idle</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>89</td>
<td>TWI</td>
<td>Static 400 µA current while using GPIOTE</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>91</td>
<td>RADIO</td>
<td>Radio performance using CSP package version</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>97</td>
<td>GPIOTE</td>
<td>High current consumption in System ON Idle mode</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>101</td>
<td>CLOCK</td>
<td>Sleep current increases after soft reset</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>102</td>
<td>RADIO</td>
<td>PAYLOAD/END events delayed or not triggered after ADDRESS</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>106</td>
<td>RADIO</td>
<td>Higher CRC error rates for some access addresses</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>107</td>
<td>RADIO</td>
<td>Immediate address match for access addresses containing MSBs 0x00</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>108</td>
<td>RAM</td>
<td>RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>109</td>
<td>DMA</td>
<td>DMA access transfers might be corrupted</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>113</td>
<td>COMP</td>
<td>Single-ended mode with external reference is not functional</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>132</td>
<td>CLOCK</td>
<td>The LFRC oscillator might not start</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>136</td>
<td>System</td>
<td>Bits in RESETREAS are set when they should not be</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>138</td>
<td>RADIO</td>
<td>Spurious emission on GPIO exceeds limits in radiated tests</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>141</td>
<td>NFCT</td>
<td>HFCLK not stopped when entering SENSE mode</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>143</td>
<td>RADIO</td>
<td>False CRC failures on specific addresses</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>146</td>
<td>CLOCK</td>
<td>LFRC frequency deviation</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>149</td>
<td>TWIM</td>
<td>First clock pulse after clock stretching may be too long or too short</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>150</td>
<td>SAADC</td>
<td>EVENT_STARTED does not fire</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>155</td>
<td>GPIOTE</td>
<td>IN event may occur more than once on input edge</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>156</td>
<td>GPIOTE</td>
<td>Some CLR tasks give unintentional behaviour</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>163</td>
<td>FICR</td>
<td>Code and RAM size fields do not match chip specification</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
3 New and inherited anomalies

Symptoms
COMP does not compare correctly.

Conditions
Always.

Consequences
COMP module is unusable.

Workaround
Execute the following code before enabling the COMP module:

```
*(volatile uint32_t *)0x40013540 = (*(volatile uint32_t *)0x10000324 & 0x00001F00) >> 8;
```

This workaround is included in MDK version 8.12.0 and later.

3.2 [15] POWER: RAM[x].POWERSET/CLR read as zero
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
RAM[x].POWERSET and RAM[x].POWERCLR read as zero, even though the RAM is on.

Conditions
Always.

Consequences
Not possible to read the RAM state using RAM[x].POWERSET and RAM[x].POWERCLR registers. Write works as it should.

Workaround
Use RAM[x].POWER to read the state of the RAM.

3.3 [20] RTC: Register values are invalid
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
RTC registers will not contain the correct/expected value if read.

Conditions
The RTC has been idle.
3 New and inherited anomalies

Consequences
RTC configuration cannot be determined by reading RTC registers.

Workaround
Execute the below code before you use RTC.

```c
NRF_CLOCK->EVENTS_LFCLKSTARTED = 0;
NRF_CLOCK->TASKS_LFCLKSTART = 1;
while (NRF_CLOCK->EVENTS_LFCLKSTARTED == 0) {}  
NRF_RTC0->TASKS_STOP = 0;
```

3.4 [31] CLOCK: Calibration values are not correctly loaded from FICR at reset

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
RCOSC32KICALLENGTH is initialized with the wrong FICR value.

Conditions
Always

Consequences
RCOSC32KICALLENGTH default value is wrong.

Workaround
Execute the following code after reset:

```c
*(volatile uint32_t *)0x4000053C = ((*(volatile uint32_t *)0x10000244) & 0x0000E000) >> 13;
```

This code is already present in the latest system_nrf52.c file.

3.5 [36] CLOCK: Some registers are not reset when expected

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
After watchdog timeout reset, CPU lockup reset, soft reset, or pin reset, the following CLOCK peripheral registers are not reset:

- CLOCK->EVENTS_DONE
- CLOCK->EVENTS_CTTO
- CLOCK->CTIV
3 New and inherited anomalies

Conditions
After watchdog timeout reset, CPU Lockup reset, soft reset, and pin reset.

Consequences
Register reset values might be incorrect. It may cause undesired interrupts in case of enabling interrupts without clearing the DONE or CTTO events.

Workaround
Clear affected registers after reset. This workaround has already been added into system_nrf52.c file. This workaround has already been added into system_nrf52840.c file present in MDK 8.11.0 or later.

3.6 [51] I2S: Aligned stereo slave mode does not work
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
Sample values for the left channel are transmitted twice (for both channels within a frame), sample values for the right channel are lost.

Conditions
CONFIG.MODE = SLAVE, CONFIG.CHANNELS = STEREO, CONFIG FORMAT = ALIGNED.

Consequences
Aligned format cannot be used for stereo transmission in Slave mode.

Workaround
None.

3.7 [54] I2S: Wrong LRCK polarity in Aligned mode
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
In Aligned mode, left and right samples are swapped.

Conditions
CONFIG FORMAT = ALIGNED

Consequences
Left and right audio channels are swapped.

Workaround
Swap left and right samples in memory.
3.8 [55] I2S: RXPTRUPD and TXPTRUPD events asserted after STOP

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

Symptoms
The RXPTRUPD event is generated when the STOP task is triggered, even though reception (RX) is disabled. Similarly, the TXPTRUPD event is generated when the STOP task is triggered, even though transmission (TX) is disabled.

Conditions
A previous transfer has been performed with RX/TX enabled, respectively.

Consequences
The indication that RXTXD.MAXCNT words were received/transmitted is false.

Workaround
Ignore the RXPTRUPD and TXPTRUPD events after triggering the STOP task. Clear these events before starting the next transfer.

3.9 [58] SPIM: An additional byte is clocked out when RXD.MAXCNT = 1

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

Symptoms
SPIM clocks out additional byte.

Conditions
RXD.MAXCNT = 1
TXD.MAXCNT <= 1

Consequences
Additional byte is redundant.

Workaround
Use the SPI module (deprecated but still available) or use the following workaround with SPIM:

```c
/**
 * @brief Work-around for transmitting 1 byte with SPIM.
 * @param spim: The SPIM instance that is in use.
 * @param ppi_channel: An unused PPI channel that will be used by the workaround.
 * @param gpiote_channel: An unused GPIOTE channel that will be used by the workaround.
 */
```
* @warning Must not be used when transmitting multiple bytes.
* @warning After this workaround is used, the user must reset the PPI channel and the GPIOTE channel before attempting to transmit multiple bytes.
*/

```c
void setup_workaround_for_ftpan_58(NRF_SPIM_Type * spim, uint32_t ppi_channel, uint32_t gpiote_channel)
{
    // Create an event when SCK toggles.
    NRF_GPIOTE->CONFIG[gpiote_channel] = (GPIOTE_CONFIG_MODE_Event <<
        GPIOTE_CONFIG_MODE_Pos)
        | (spim->PSEL.SCK <<
        GPIOTE_CONFIG_PSEL_Pos)
        | (GPIOTE_CONFIG_POLARITY_Toggle <<
        GPIOTE_CONFIG_POLARITY_Pos);

    // Stop the spim instance when SCK toggles.
    NRF_PPI->CH[ppi_channel].EEP = (uint32_t)&NRF_GPIOTE->EVENTS_IN[gpiote_channel];
    NRF_PPI->CH[ppi_channel].TEP = (uint32_t)&spim->TASKS_STOP;
    NRF_PPI->CHENSET = 1U << ppi_channel;

    // The spim instance cannot be stopped mid-byte, so it will finish
    // transmitting the first byte and then stop. Effectively ensuring
    // that only 1 byte is transmitted.
}
```

### 3.10 [64] NFCT: Only full bytes can be received or transmitted, but supports 4-bit frame transmit

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

#### Symptoms

Data bits are not transmitted, or appear to not be received, if the Frame length is not a multiple of 8 bits (i.e. Frame includes data bits).

#### Conditions

Frame length is not a multiple of 8 bits (bytes only). Exception: 4-bit frame transmit supported.

#### Consequences

Partial bytes cannot be transferred:

- TXD.AMOUNT.TXDATABITS must be 0
- RXD.AMOUNT.RXDATABITS must be 0

#### Workaround

None
3.11 [66] TEMP: Linearity specification not met with default settings

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

**Symptoms**

TEMP module provides non-linear temperature readings over the specified temperature range.

**Conditions**

Always

**Consequences**

TEMP module returns out of spec temperature readings.

**Workaround**

Execute the following code after reset:

```c
NRF_TEMP->A0 = NRF_FICR->TEMP.A0;
NRF_TEMP->A1 = NRF_FICR->TEMP.A1;
NRF_TEMP->A2 = NRF_FICR->TEMP.A2;
NRF_TEMP->A3 = NRF_FICR->TEMP.A3;
NRF_TEMP->A4 = NRF_FICR->TEMP.A4;
NRF_TEMP->A5 = NRF_FICR->TEMP.A5;
NRF_TEMP->B0 = NRF_FICR->TEMP.B0;
NRF_TEMP->B1 = NRF_FICR->TEMP.B1;
NRF_TEMP->B2 = NRF_FICR->TEMP.B2;
NRF_TEMP->B3 = NRF_FICR->TEMP.B3;
NRF_TEMP->B4 = NRF_FICR->TEMP.B4;
NRF_TEMP->B5 = NRF_FICR->TEMP.B5;
NRF_TEMP->T0 = NRF_FICR->TEMP.T0;
NRF_TEMP->T1 = NRF_FICR->TEMP.T1;
NRF_TEMP->T2 = NRF_FICR->TEMP.T2;
NRF_TEMP->T3 = NRF_FICR->TEMP.T3;
NRF_TEMP->T4 = NRF_FICR->TEMP.T4;
```

This code is already present in the latest system_nrf52.c file and in the system_nrf52840.c file released in MDK 8.12.0.

3.12 [67] NFCT,PPI: Some events cannot be used with the PPI

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

**Symptoms**

The following NFCT events do not trigger tasks when used with the PPI:

- EVENTS_AUTOCOLRESSTARTED
- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED
Conditions
PPI is used to trigger peripheral tasks using the NFCT events.

Consequences
The PPI cannot be used to trigger tasks using the following NFCT events:
- EVENTS_AUTOCOLRESSTARTED
- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

Workaround
The EVENTS_AUTOCOLRESSTARTED cannot be used with the PPI.
Subtract an offset of 0x04 while configuring the PPI event end points for the following NFCT events:
- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

Examples:

```
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_COLLISION) - 0x04;
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_SELECTED) - 0x04;
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_STARTED) - 0x04;
```

3.13 [68] CLOCK: EVENTS_HFCLKSTARTED can be generated before HFCLK is stable
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
EVENTS_HFCLKSTARTED may come before HFXO is started.

Conditions
When using a 32 MHz crystal with start-up longer than 400 µs.

Consequences
Performance of radio and peripheral requiring HFXO will be degraded until the crystal is stable.

Workaround
32 MHz crystal oscillator startup time must be verified by the user. If the worst-case startup time is shorter than 400 µs, no workaround is required. If the startup time can be longer than 400 µs, the software must ensure, using a timer, that the crystal has had enough time to start up before using peripherals that require the HFXO. The Radio requires the HFXO to be stable before use. The ADC, TIMERS, and TEMP sensor for example can use the HFXO as a reference for improved accuracy.
3.14 [72] NFCT,PPI: TASKS_ACTIVATE cannot be used with the PPI
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

**Symptoms**
The NFCT peripheral does not get activated when the PPI is configured to trigger TASKS_ACTIVATE on any event.

**Conditions**
Always

**Consequences**
The TASKS_ACTIVATE cannot be used with the PPI.

**Workaround**
None

3.15 [74] SAADC: Started events fires prematurely
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

**Symptoms**
False EVENTS_STARTED

**Conditions**
TACQ <= 5 µs

**Consequences**
The EVENTS_STARTED can come when not expected

**Workaround**
The module must be fully configured before it is enabled, and the TACQ configuration must be the last configuration set before ENABLE.

3.16 [75] MWU: Increased current consumption
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

**Symptoms**
Increased current consumption in System ON IDLE.
3 New and inherited anomalies

Conditions
When MWU is enabled.

Consequences
Increased current consumption in System ON IDLE.

Workaround
Do not use MWU or disable MWU before WFE/WFI, enable it on IRQ.

3.17 [76] LPCOMP: READY event is set sooner than it should
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
May receive unexpected events and wakeups from LPCOMP.

Conditions
LPCOMP is configured to send an event or to wake up the chip. LPCOMP.TASKS_START task is set and LPCOMP.EVENTS_READY event has been received.

Consequences
Unpredictable system behavior caused by falsely triggered events and wakeups.

Workaround
Use the following configuration sequence.
1. Configure the LPCOMP to send an event or wake up the chip, but do not enable any PPI channels or IRQ to be triggered from the LPCOMP events.
2. Trigger the LPCOMP.TASKS_START task and wait for the LPCOMP.EVENTS_READY event.
3. After receiving the LPCOMP.EVENTS_READY event wait for 115 µs.
4. After 115 µs, clear the LPCOMP.EVENTS_DOWN, LPCOMP.EVENTS_UP, and LPCOMP.EVENTS_CROSS events.
   LPCOMP is now ready to be used.

3.18 [77] CLOCK: RC oscillator is not calibrated when first started
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
The LFCLK RC oscillator frequency can have a frequency error of up to -25 to +40% after reset. A +/- 2% error is stated in the Product Specification.

Conditions
Always
Consequences
The LFCLK RC oscillator frequency is inaccurate.

Workaround
Calibrate the LFCLK RC oscillator before its first use after a reset.

3.19 [78] TIMER: High current consumption when using timer STOP task only
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
Increased current consumption when the timer has been running and the STOP task is used to stop it.

Conditions
The timer has been running (after triggering a START task) and then it is stopped using a STOP task only.

Consequences
Increased current consumption

Workaround
Use the SHUTDOWN task after the STOP task or instead of the STOP task.

3.20 [79] NFCT: A false EVENTS_FIELDDETECTED event occurs after the field is lost
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
A false EVENTS_FIELDDETECTED event occurs.

Conditions
The task TASK_SENSE is triggered within 270 µs of the event EVENTS_FIELDLOST.

Consequences
EVENTS_FIELDDETECTED will occur after a field is lost. (SHORT between eventfieldlost and taskSense should not be used since a false fieldDetected event will occur from using the task.)

Workaround
• Wait 170 µs after an EVENTS_FIELDLOST event before triggering TASK_SENSE for temperatures ≥ 0°C.
• Wait 270 µs after an EVENTS_FIELDLOST event before triggering TASK_SENSE for temperatures < 0°C.

Important: This anomaly was changed compared to the original publication.
3.21 [81] GPIO: PIN_CNF is not retained when in debug interface mode

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

**Symptoms**

GPIO pin configuration is reset on wakeup from System OFF.

**Conditions**

The system is in debug interface mode.

**Consequences**

GPIO state unreliable until PIN_CNF is reconfigured.

3.22 [83] TWIS: STOPPED event occurs twice if the STOP task is triggered during a transaction

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

**Symptoms**

STOPPED event is set after clearing it.

**Conditions**

The STOP task is triggered during a transaction.

**Consequences**

STOPPED event occurs twice: When the STOP task is fired and when the master issues a stop condition on the bus. This could provoke an extra interrupt or a failure in the TWIS driver.

**Workaround**

The last STOPPED event must be accounted for in software.

3.23 [84] COMP: ISOURCE not functional

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

**Symptoms**

The programmable current source (ISOURCE) has too high variation. Variance over temp is >20 times specified nominal value.

**Conditions**

Always.
3.24 [86] SAADC: Triggering START task after offset calibration may write a sample to RAM
This anomaly applies to IC Rev. Rev 1, build codes QFAB-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
The first sample in the result buffer is incorrect, and will be present although the SAMPLE task has never been issued.

Conditions
The START task is triggered after performing calibration (through the CALIBRATEOFFSET task).

Consequences
Incorrect sample data in the result buffer.

Workaround
Calibration should follow the pattern STOP -> STOPPED -> CALIBRATEOFFSET -> CALIBRATEDONE -> STOP -> STOPPED -> START.

3.25 [87] CPU: Unexpected wake from System ON Idle when using FPU
This anomaly applies to IC Rev. Rev 1, build codes QFAB-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
The CPU is unexpectedly awoken from System ON Idle.

Conditions
The FPU has been used.

Consequences
The CPU is awoken from System ON Idle.

Workaround
The FPU can generate pending interrupts just like other peripherals, but unlike other peripherals there are no INTENSET, INTENCLR registers for enabling or disabling interrupts at the peripheral level. In order to prevent unexpected wake-up from System ON Idle, add this code before entering sleep:
3.26 [88] WDT: Increased current consumption when configured to pause in System ON idle

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

**Symptoms**

Using the mode where watchdog is paused in CPU Idle, the current consumption jumps from 3 µA to 400 µA.

**Conditions**

When we enable WDT with the CONFIG option to pause when CPU sleeps:

```c
NRF_WDT->CONFIG = (WDT_CONFIG_SLEEP_Pause<<WDT_CONFIG_SLEEP_Pos);
```

**Consequences**

Reduced battery life

**Workaround**

Do not enter System ON IDLE within 125 µs after reloading the watchdog.

3.27 [89] TWI: Static 400 µA current while using GPIOTE

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

**Symptoms**

Static current consumption between 400 µA to 450 µA when using TWI in combination with GPIOTE.

**Conditions**

- GPIOTE is configured in event mode
- TWI utilizes EasyDMA

**Consequences**

Current consumption higher than specified

**Workaround**

Turn the TWI off and back on after it has been disabled. To do so: If TWI0 is used,
If TWI1 is used,

```c
*(volatile uint32_t *)0x40004FFC = 0;
*(volatile uint32_t *)0x40004FFC;
*(volatile uint32_t *)0x40004FFC = 1;
```

write 0 followed by a 1 to the POWER register (address 0xFFC) of the TWI that needs to be disabled. Reconfiguration of TWI is required before next usage.

### 3.28 [91] RADIO: Radio performance using CSP package version

This anomaly applies to IC Rev. Rev 1, build codes CIAA-B00. It was inherited from the previous IC revision Engineering C.

**Symptoms**

WLCSP package has reduced receiver sensitivity compared to QFN packages in LDO and DCDC regulator modes.

**Conditions**

- Average Sensitivity over all channels degraded in LDO mode by 2 dB.
- Average Sensitivity over all channels degraded in DCDC mode by 4 dB.

**Consequences**

Reduced receiver sensitivity.

**Workaround**

None.

### 3.29 [97] GPIOTE: High current consumption in System ON Idle mode

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00. It was inherited from the previous IC revision Engineering C.

**Symptoms**

High current consumption (<20 µA) in System ON Idle mode.

**Conditions**

GPIOTE used with one or more channels in input mode.

**Consequences**

Higher current consumption.
3.30 [101] CLOCK: Sleep current increases after soft reset
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
Sleep current with LFXO active is 0.5 µA higher than expected.

Conditions
Low frequency crystal oscillator is active, due to use of RTC or WDT, and a soft-reset is issued or a CPU lock-up reset occurs.

Consequences
Increased sleep current.

Workaround
None.

3.31 [102] RADIO: PAYLOAD/END events delayed or not triggered after ADDRESS
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
After the ADDRESS event, the PAYLOAD/END events might not trigger until another packet is received with the same access address. The frequency at which this occurs is low (<0.1% of packets).

Conditions
BLE and Nordic proprietary radio mode. Radio receive mode.

Consequences
The radio remains in receive mode until the next packet is received. Both packets are lost.

Workaround
Use one of the following workarounds:

• Use SoftDevice s132_nrf52_4.0.2 or later and the ESB and Gazell libraries of SDK v14.0.0 or later. These implementations prevent the radio from remaining in receive mode when a packet is not received.
• Apply the following code before triggering the RXEN task:
3 New and inherited anomalies

This code will reduce sensitivity with 3 dB.

### 3.32 [106] RADIO: Higher CRC error rates for some access addresses

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

**Symptoms**

Payload in RX is corrupted.

**Conditions**

BLE and Nordic proprietary radio mode. 4 and 5 byte addresses. 1 in 1600 (<0.07%) randomly generated BLE addresses and 1 in 1200 (<0.09%) randomly generated proprietary addresses are affected.

**Consequences**

The radio reports up to 30% CRC error rate for packets being received when affected access addresses are used. For BLE, new access addresses are generated on each connection so the symptom is rare and not persistent.

**Workaround**

Use one of the following workarounds:

- Use SoftDevice s132_nrf52_4.0.2 or later and the ESB and Gazell libraries of SDK v14.0.0 or later to avoid higher CRC error rate.

  The S132 SoftDevice detects when affected access addresses are being used in a connection and applies the following workaround resulting in 3 dB reduced sensitivity for approximately 0.1% of connections. The ESB and Gazell libraries apply the following workaround for all addresses.

- Apply the following code before triggering the RXEN task:

  ```c
  *(volatile uint32_t *) 0x40001774 = (((volatile uint32_t *)
  0x40001774) & 0xfffffffe) | 0x01000000;
  ```

  This code will reduce sensitivity with 3 dB.

### 3.33 [107] RADIO: Immediate address match for access addresses containing MSBs 0x00

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

**Symptoms**

Loss of connection.

**Conditions**

Nordic proprietary radio mode with 4 and 5 byte addresses with certain combinations of 0 in the access address. BLE addresses are not affected.
Consequences

100% packet error rate.

Workaround

Either use the ESB and Gazell libraries of SDK v14.0.0 or later, or avoid using access addresses in the following pattern (where X is don’t care):

<table>
<thead>
<tr>
<th>ADDRLEN=5</th>
<th>BASE0</th>
<th>PREFIX0 = 0xXXXXXXX0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BASE1</td>
<td>= 0x0000XXXX, PREFIX0 = 0xXXXXX0XX</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x0000XXXX, PREFIX0 = 0xXXXX00XX</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x0000XXXX, PREFIX0 = 0xXX00XXXX</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x0000XXXX, PREFIX0 = 0x00XXXXXX</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x0000XXXX, PREFIX1 = 0xXXXXXX00</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x0000XXXX, PREFIX1 = 0xXXXX00XX</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x0000XXXX, PREFIX1 = 0xXX00XXXX</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x0000XXXX, PREFIX1 = 0x00XXXXXX</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ADDRLEN=4</th>
<th>BASE0</th>
<th>PREFIX0 = 0xXXXXXXX0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BASE1</td>
<td>= 0x00XXXXXX, PREFIX0 = 0xXXXXXX00</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x00XXXXXX, PREFIX0 = 0xXXXX00XX</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x00XXXXXX, PREFIX0 = 0xXX00XXXX</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x00XXXXXX, PREFIX0 = 0x00XXXXXX</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x00XXXXXX, PREFIX1 = 0xXXXXXX00</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x00XXXXXX, PREFIX1 = 0xXXXX00XX</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x00XXXXXX, PREFIX1 = 0xXX00XXXX</td>
<td></td>
</tr>
<tr>
<td>BASE1</td>
<td>= 0x00XXXXXX, PREFIX1 = 0x00XXXXXX</td>
<td></td>
</tr>
</tbody>
</table>

3.34 [108] RAM: RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

Symptoms

RAM not correctly retained.

Conditions

System ON Idle mode or System OFF is used with parts or all RAM retained.

Consequences

RAM not correctly retained.

Workaround

Apply the following code after any reset:

```c
*(volatile uint32_t *)0x40000EE4 = (*(volatile uint32_t *)0x10000258 & 0x0000004F);
```

This workaround is implemented in MDK version 8.9.0 and newer version. This workaround increases the I_RAM current per 4 KB section from 20nA to 30nA.
3.35 [109] DMA: DMA access transfers might be corrupted
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
The first byte sent out by the peripheral is sometimes wrong.

Conditions
System enters IDLE and stops the 64 MHz clock at the same time as the peripheral that is using DMA is started.
This problem affects the peripherals PWM, SPI/S, SPI/M, TWI/S, UART/E, and TWI/M.

Consequences
Wrong data sent to external device.

Workaround
Workarounds will be incorporated into SDK v13.0.0. See the following document for a description of the workarounds:

3.36 [113] COMP: Single-ended mode with external reference is not functional
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
COMP output is not correct.

Conditions
COMP is used in single-ended mode with external reference.

Consequences
COMP cannot be used in this mode.

Workaround
None.

3.37 [132] CLOCK: The LFRC oscillator might not start
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.
Symptoms
The LFRC oscillator does not start and the LFCLKSTARTED event is not triggered.

Conditions
The LFRC oscillator is started in the window [66 µs, 138 µs] after the LFRC oscillator has stopped.

Consequences
The LFRC oscillator might become non-functional until it is reset.

Workaround
Delay starting the LFRC oscillator if it was last stopped [66 µs, 138 µs] ago.

3.38 [136] System: Bits in RESETREAS are set when they should not be
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
After pin reset, RESETREAS bits other than RESETPIN might also be set.

Conditions
A pin reset has triggered.

Consequences
If the firmware evaluates RESETREAS, it might take the wrong action.

Workaround
When RESETREAS shows a pin reset (RESETPIN), ignore other reset reason bits.

Important: RESETREAS bits must be cleared between resets.

Apply the following code after any reset:

```c
if (NRF_POWER->RESETREAS & POWER_RESETREAS_RESETPIN_Msk) {
    NRF_POWER->RESETREAS = ~POWER_RESETREAS_RESETPIN_Msk;
}
```

This workaround is implemented in MDK version 8.13.0 and later.

3.39 [138] RADIO: Spurious emission on GPIO exceeds limits in radiated tests
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00.

Symptoms
Spurious emission in RX mode can exceed ETSI limits.
3.40 [141] NFCT: HFCLK not stopped when entering SENSE mode
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
Higher current consumption than specified in SENSE mode.

Conditions
Going from active mode to SENSE mode.

Consequences
Higher current consumption in SENSE mode than specified.

Workaround
Power cycle the NFCT using the POWER register, then issue the SENSE task to enter SENSE mode.

3.41 [143] RADIO: False CRC failures on specific addresses
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

Symptoms
100% CRC failure rate even if the payload is received correctly.

Conditions
Nordic proprietary radio mode. CRCCNF.SKIPADDR = 0. CRC calculation includes the address field.
Logical address 0 and logical address 1 to 7 have the same BASE address MSBs configured.

```
ADDRLEN=5
BASE0 = 0xAAAAXXXX
BASE1 = 0xAAAAXXXX
ADDRLENLEN=4
BASE0 = 0xAAAXXXXX
BASE1 = 0xAAAXXXXX
```

AND logical address 0 and one of the logical addresses 1 to 7 have the same PREFIX value configured.
The issue is present regardless of which logical address is enabled in RXADDRESSES.

**Consequences**

If receiving on logical address 0, the address is reconstructed incorrectly for CRC calculation, resulting in CRCSTATUS.CRCError being returned. However, the received payload bytes are correct. Packet error rate 100 percent. RXMATCH shows the wrong logical address.

**Workaround**

Use one of the following workarounds:

- Use the ESB and Gazell libraries of SDK v14.0.0 or later.
  
  This implementation applies the following workaround.

- Set bit 16 in RXADDRESSES to 1.

- Apply the following code before triggering the RXEN task:

  ```c
  *(volatile uint32_t *) 0x40001774 = (*((volatile uint32_t *)
  0x40001774) & 0xfffffffe) | 0x01000000;
  ```

  This code will reduce sensitivity with 3 dB.

---

**3.42 [146] CLOCK: LFRC frequency deviation**

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

**Symptoms**

The frequency tolerance (fTOL_CAL_LFRC) of the LFRC oscillator is exceeding 250 ppm.

**Conditions**

Always.

**Consequences**

Timers using LFRC are not as precise as described in the specification.

**Workaround**

Account for a frequency tolerance of 500 ppm when using the LFRC oscillator.

---

**3.43 [149] TWIM: First clock pulse after clock stretching may be too long or too short**

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.

It was inherited from the previous IC revision Engineering C.

**Symptoms**

When the TWI slave exits a clock stretching state, the first clock pulse from the master is too long or too short. The following deviations from the normal clock pulse length can occur:
### 3.44 [150] SAADC: EVENT_STARTED does not fire

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00. It was inherited from the previous IC revision Engineering C.

**Symptoms**

EVENT_STARTED does not fire.

**Conditions**

ADC started (TASKS_START) with PPI task. Any channel configured to TACQ $\leq 5$ µs.

**Consequences**

ADC cannot be started (TASKS_START) with PPI if TACQ $\leq 5$ µs.

**Workaround**

Use TAQC $> 5$ µs when starting ADC from PPI.

### 3.45 [155] GPIOTE: IN event may occur more than once on input edge

This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00. It was inherited from the previous IC revision Engineering C.

**Symptoms**

IN event occurs more than once on an input edge.

**Conditions**

Input signal edges are closer together than 1.3 µs or $\geq 750$ kHz for a periodic signal.
Consequences
Tasks connected through PPI or SHORTS to this event might be triggered twice.

Workaround
Apply the following code when any GPIOTE channel is configured to generate an IN event on edges that can occur within 1.3 µs of each other:

```c
*(volatile uint32_t *)(NRF_GPIOTE_BASE + 0x600 + (4 * GPIOTE_CH_USED)) = 1;
```

**Important:** A clock is kept on by the workaround and must be reverted to avoid higher current consumption when GPIOTE is not in use, using the following code:

```c
*(volatile uint32_t *)(NRF_GPIOTE_BASE + 0x600 + (4 * GPIOTE_CH_USED)) = 0;
```

3.46 [156] GPIOTE: Some CLR tasks give unintentional behavior
This anomaly applies to IC Rev. Rev 1, build codes QFAA-B00, QFAB-B00, CIAA-B00.
It was inherited from the previous IC revision Engineering C.

Symptoms
One of the following:

- Current consumption is high when entering IDLE.
- Latency for detection changes on inputs connected to GPIOTE channels becoming longer that expected.

Conditions
Using the following tasks:

<table>
<thead>
<tr>
<th>Address</th>
<th>GPIOTE task</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x060</td>
<td>TASK_CLR[0]</td>
</tr>
<tr>
<td>0x064</td>
<td>TASK_CLR[1]</td>
</tr>
<tr>
<td>0x068</td>
<td>TASK_CLR[2]</td>
</tr>
<tr>
<td>0x06C</td>
<td>TASK_CLR[3]</td>
</tr>
<tr>
<td>0x070</td>
<td>TASK_CLR[4]</td>
</tr>
<tr>
<td>0x074</td>
<td>TASK_CLR[5]</td>
</tr>
<tr>
<td>0x078</td>
<td>TASK_CLR[6]</td>
</tr>
<tr>
<td>0x07C</td>
<td>TASK_CLR[7]</td>
</tr>
</tbody>
</table>

Consequences
High current consumption or too long time from external event to internal triggering of PPI event and/or IRQ from GPIOTE.
Using \texttt{TASK\_CLR[n]} for even values of \(n\) has the side effect of setting the system in constant latency mode (see \texttt{POWER->TASKS\_CONSTLAT}). Using \texttt{TASK\_CLR[n]} for odd values of \(n\) has the side effect of setting the system in low power mode (see \texttt{POWER->TASKS\_LOWPOWER}).

**Workaround**

To set the system back in the mode it was before using the \texttt{TASK\_CLR[n]}, triggering of tasks with even \(n\) must be followed by triggering any of the \texttt{TASK\_CLR} with odd \(n\) and vice versa.

### 3.47 [163] FICR: Code and RAM size fields do not match chip specification

This anomaly applies to IC Rev. Rev 1, build codes QFAB-B00.

**Symptoms**

FICR values CODESIZE and INFO.RAM does not contain correct values.

**Conditions**

Always.

**Consequences**

None.

**Workaround**

None.